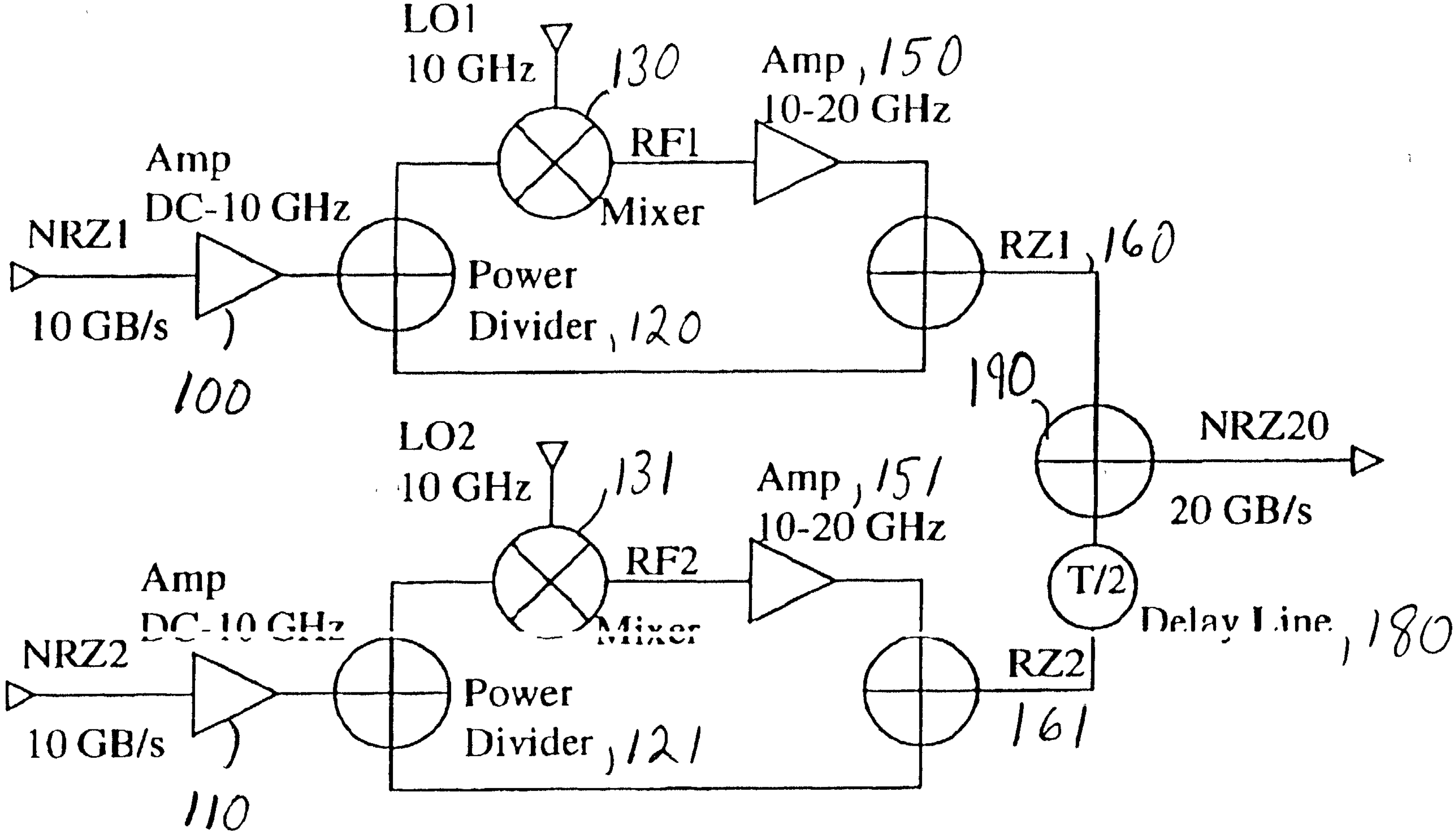
FIGURE 1



LO1
10 GHz
130
RF1
Mixer
Amp , 150
10-20 GHz
Amp
DC-10 GHz
NRZ1
10 GB/s
100
Power
Divider , 120
RZ1 , 160
190
NRZ20
20 GB/s
T/2
Delay Line , 180
LO2
10 GHz
131
RF2
Mixer
Amp , 151
10-20 GHz
Amp
DC-10 GHz
NRZ2
10 GB/s
110
Power
Divider , 121
RZ2
161

FIGURE 2

		Clock	
		1	0
Data	1	1	0
	0	0	0

- **Logic Diagram resulting from And gate**
- **Two output states**

FIGURE 3

		Clock	
		1	-1
Data	1	1	-1
	0	0	0

- **Logic diagram resulting from mixer**
- **Three output states**

- **Reduce to two states by adding original data stream**
- **Two output levels**
- **Effects NRZ to RZ conversion**

		Clock							
		1	-1						
Data	1	1	1	:	Data	1	=	1	0
	0	0	0			0		0	0

FIGURE 4